



# PRODUCTION METHOD FOR SILICON WAFER AND SILICON WAFER

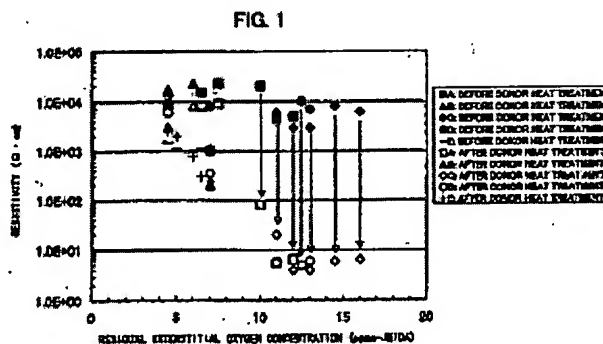
**Patent number:** EP1087041  
**Publication date:** 2001-03-28  
**Inventor:** ABE TAKAO [JP]; AIHARA KEN [JP]; AKIYAMA SHOJI [JP]; IGARASHI TETSUYA [JP]; QU WEIFENG [JP]; HAYAMIZU YOSHINORI [JP]; SAITO SHIGERU [JP]  
**Applicant:** SHINETSU HANDOTAI KK [JP]  
**Classification:**  
 - international: C30B29/06; H01L21/322; H01L27/12  
 - european: C30B15/00; H01L21/322B8  
**Application number:** EP20000905367 20000225  
**Priority number(s):** WO2000JP01124 20000225; JP19990070963 19990316; JP19990241370 19990827

Also published as:

 WO0055397 (A1)  
 US6544656 (B1)

## Abstract of EP1087041

A silicon wafer is produced by growing a silicon single crystal ingot having a resistivity of 100 OMEGA .cm or more and an initial interstitial oxygen concentration of 10 to 25 ppma by the Czochralski method, processing the silicon single crystal ingot into a wafer, and subjecting the wafer to an oxygen precipitation heat treatment so that a residual interstitial oxygen concentration in the wafer should become 8 ppma or less. A silicon wafer produced as described above shows little decrease in resistivity even after a heat treatment in device production etc. Further, if a silicon wafer is produced and heat-treated so that the wafer should have the above-defined initial interstitial oxygen concentration and residual interstitial oxygen concentration, slip dislocations in a subsequent heat treatment process are prevented irrespective of resistivity. Furthermore, by forming an epitaxial layer on a surface of a silicon wafer of the present invention, a high resistivity epitaxial wafer can be produced, which is free from slip dislocations etc. and can be used for various devices.



Data supplied from the esp@cenet database - Worldwide